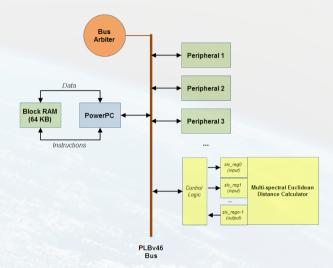
Design of improved hardware configurations for spaceborne FPGA-based architectures A. Cristo, K. Fisher, A. J. Gualtieri, R. M. Pérez, P. Martínez

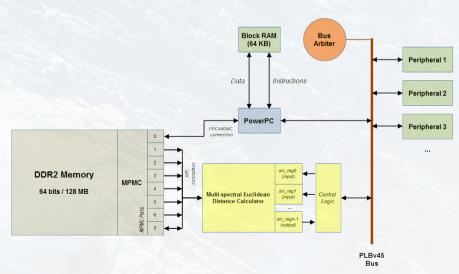
- The SpaceCube system is being developed by engineers of NASA Goddard Space Flight Center. It is based on Virtex-5 commercial FPGAs, so it can rival the performance and capability of existing flight processors.
- Two modular circuits to calculate a simple operation, the multi-spectral Euclidean distance, have been designed (sequential and parallel).
- Both circuits have been added in a hardware communication system with two different configurations (Based on a central bus and based in shared 64-bit DDR2 memories through NPI connections).
- Results show that the way the methodology is designed and implemented in the FPGA is important to get high performance, but the way the global hardware and communication system are developed also is.

Processor	Design Bus		Design Memories	
	(Sequential)	(Parallel)	(Sequential)	(Parallel)
1X	1.5X	1.48X	10.07X	11.04X

Speed-up for the sequential and parallel circuits, resident in the hardware system configurations proposed.



Configuration based on central bus.



Configuration based on DDR2 shared memories.